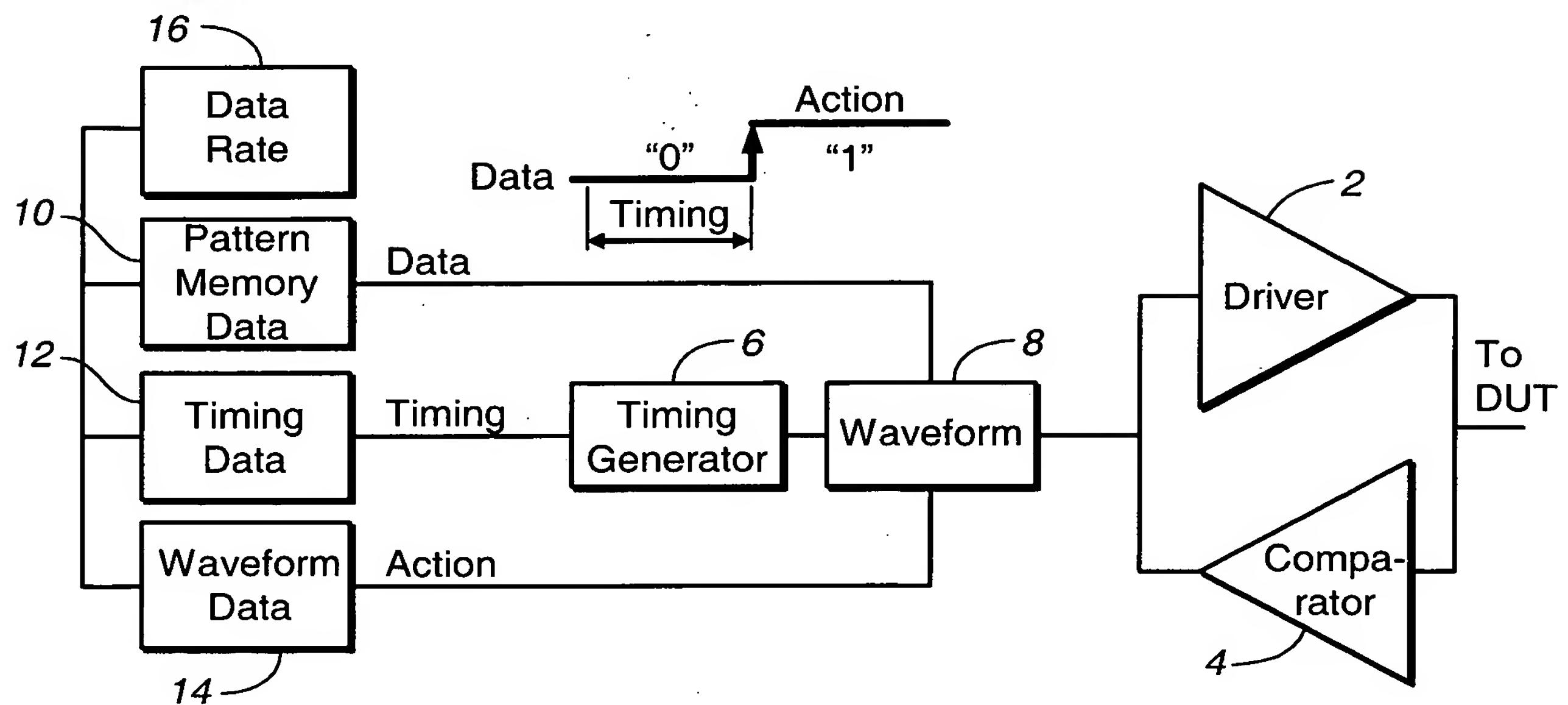




Title: METHOD AND STRUCTURE TO DEVELOP
 A TEST PROGRAM FOR SEMICONDUCTOR
 INTEGRATED CIRCUITS
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Action = Pattern Data * Timing Data (Limited by TimeSet) * Waveset * Drive

FIG._1

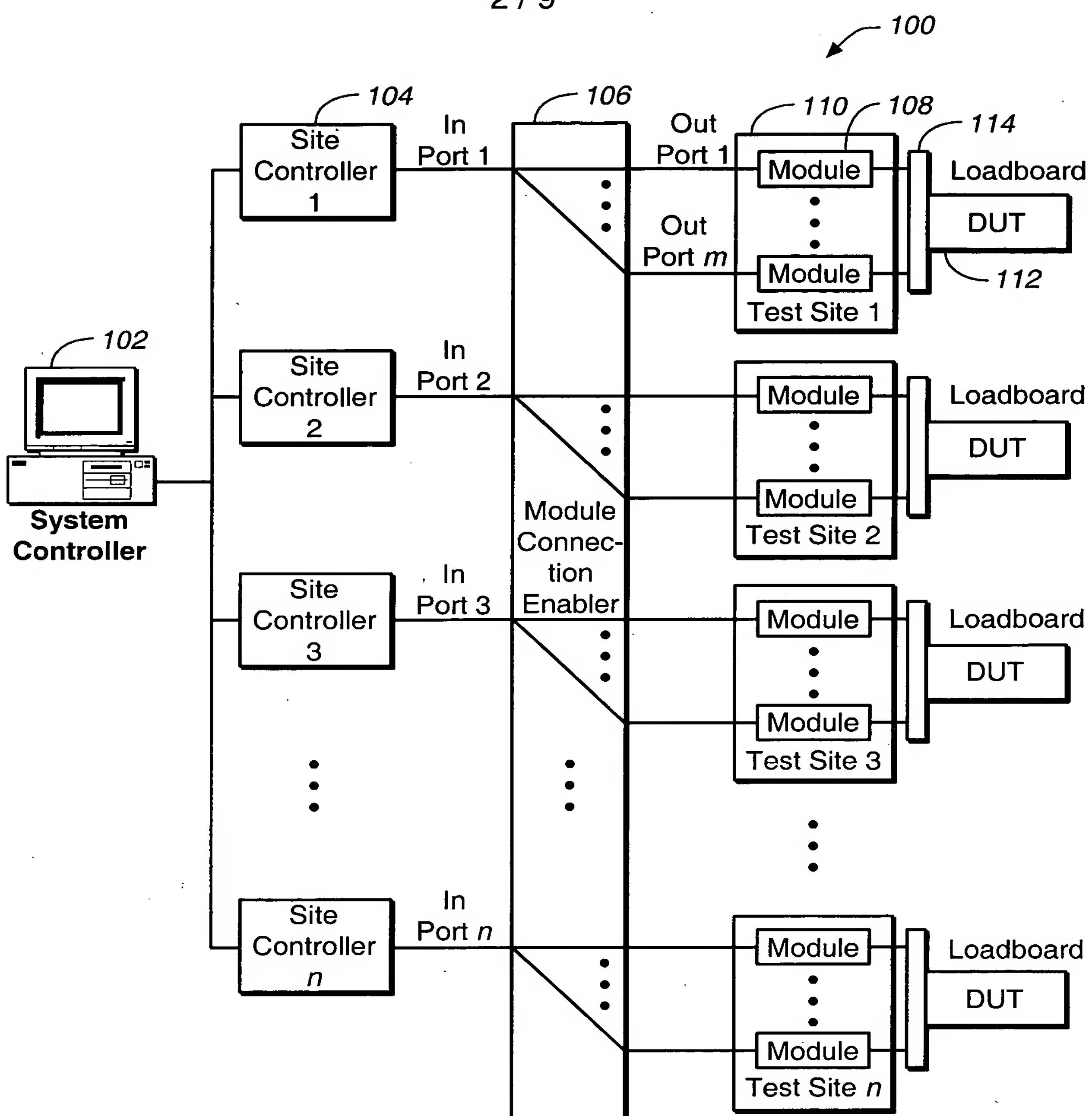


FIG._2

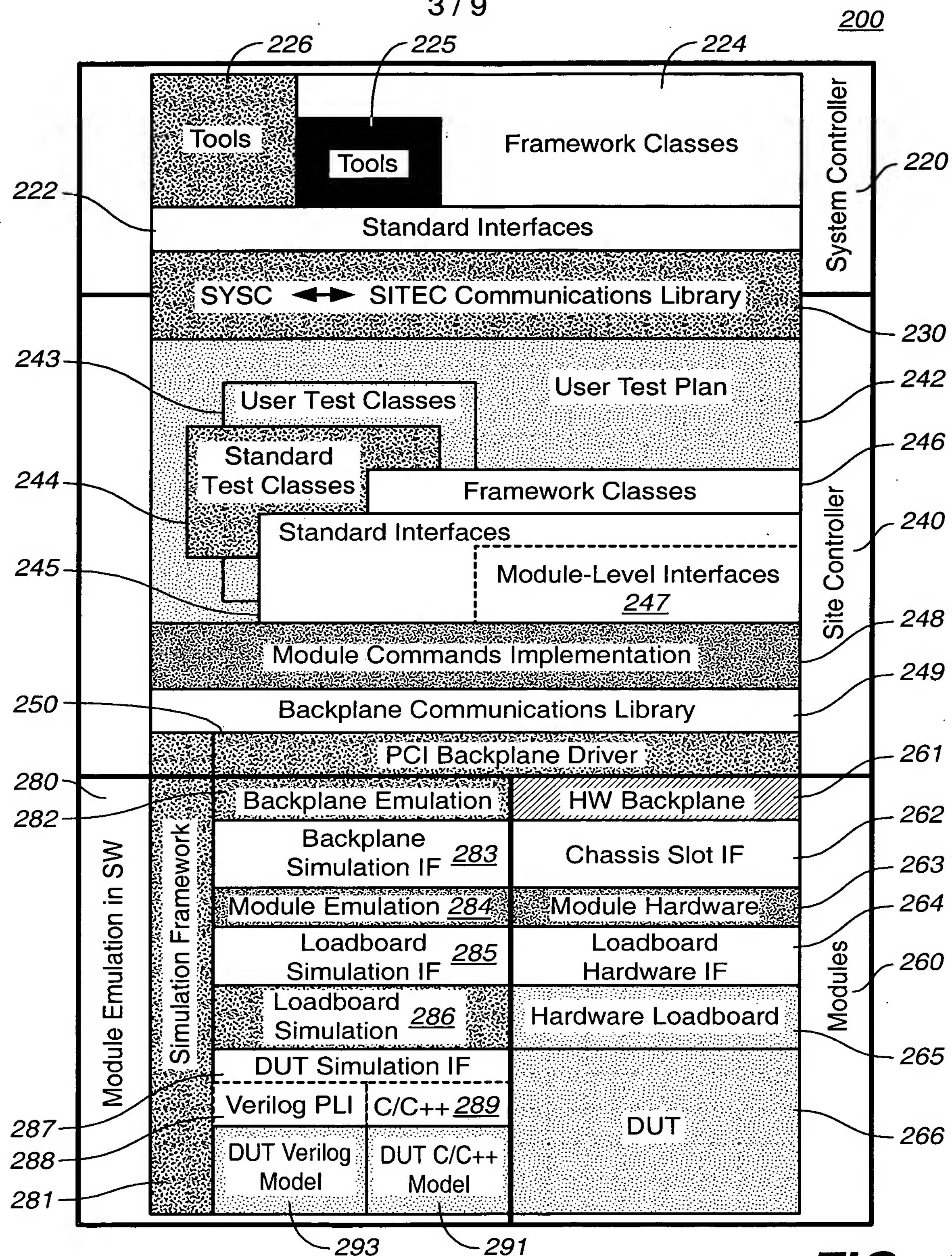
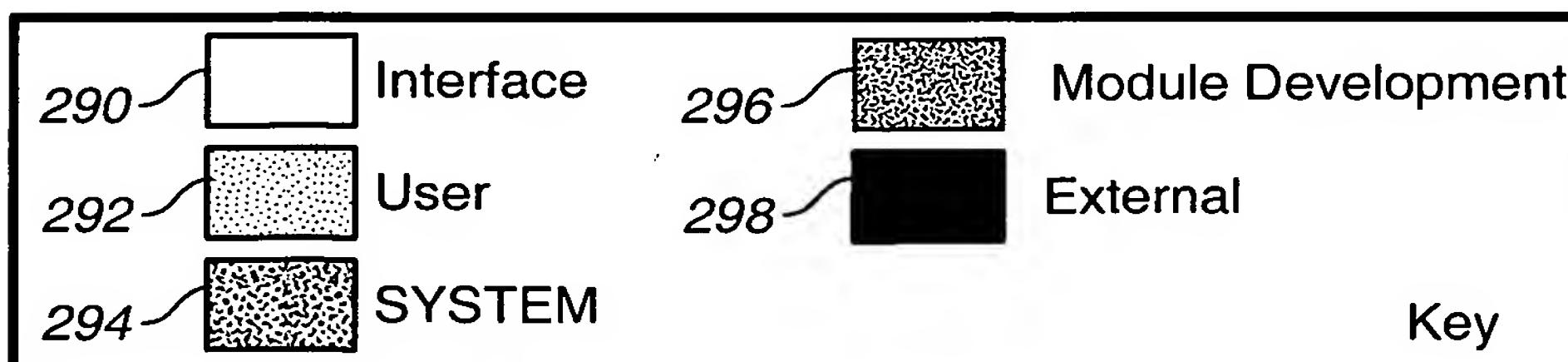


FIG._3



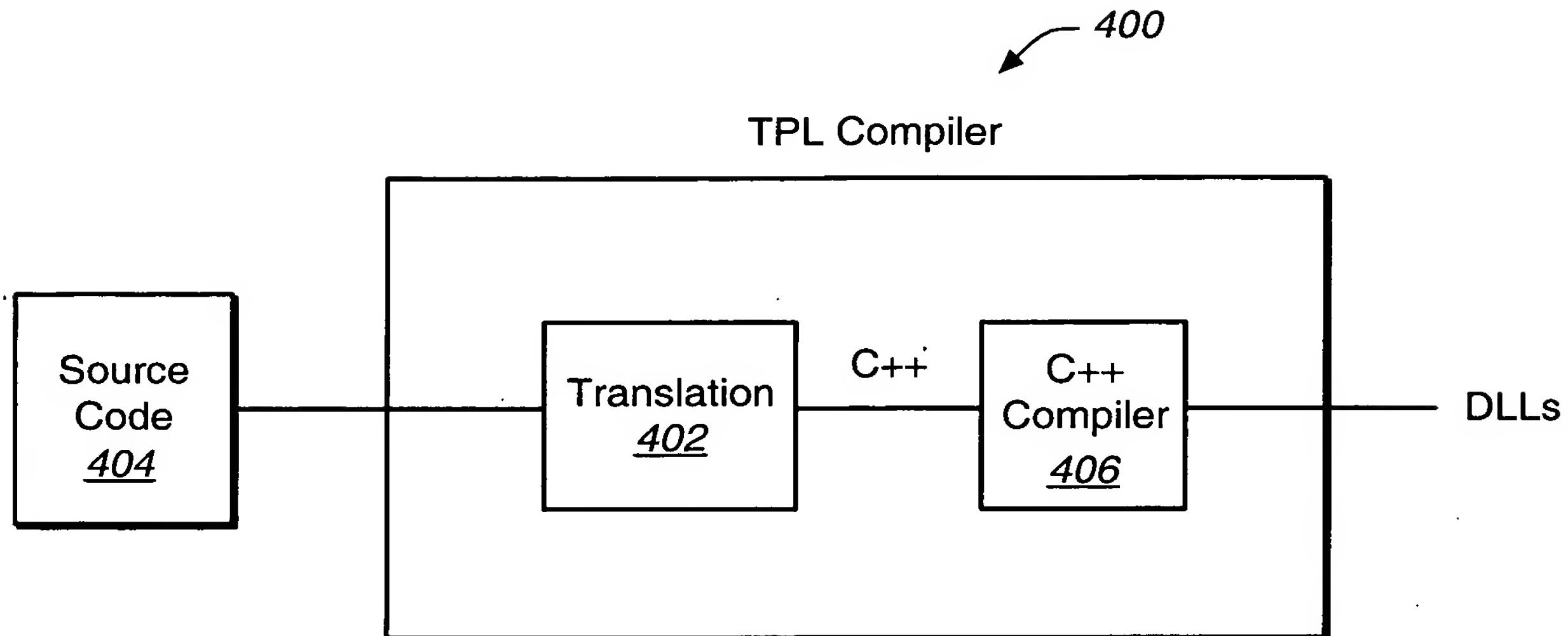


FIG._4

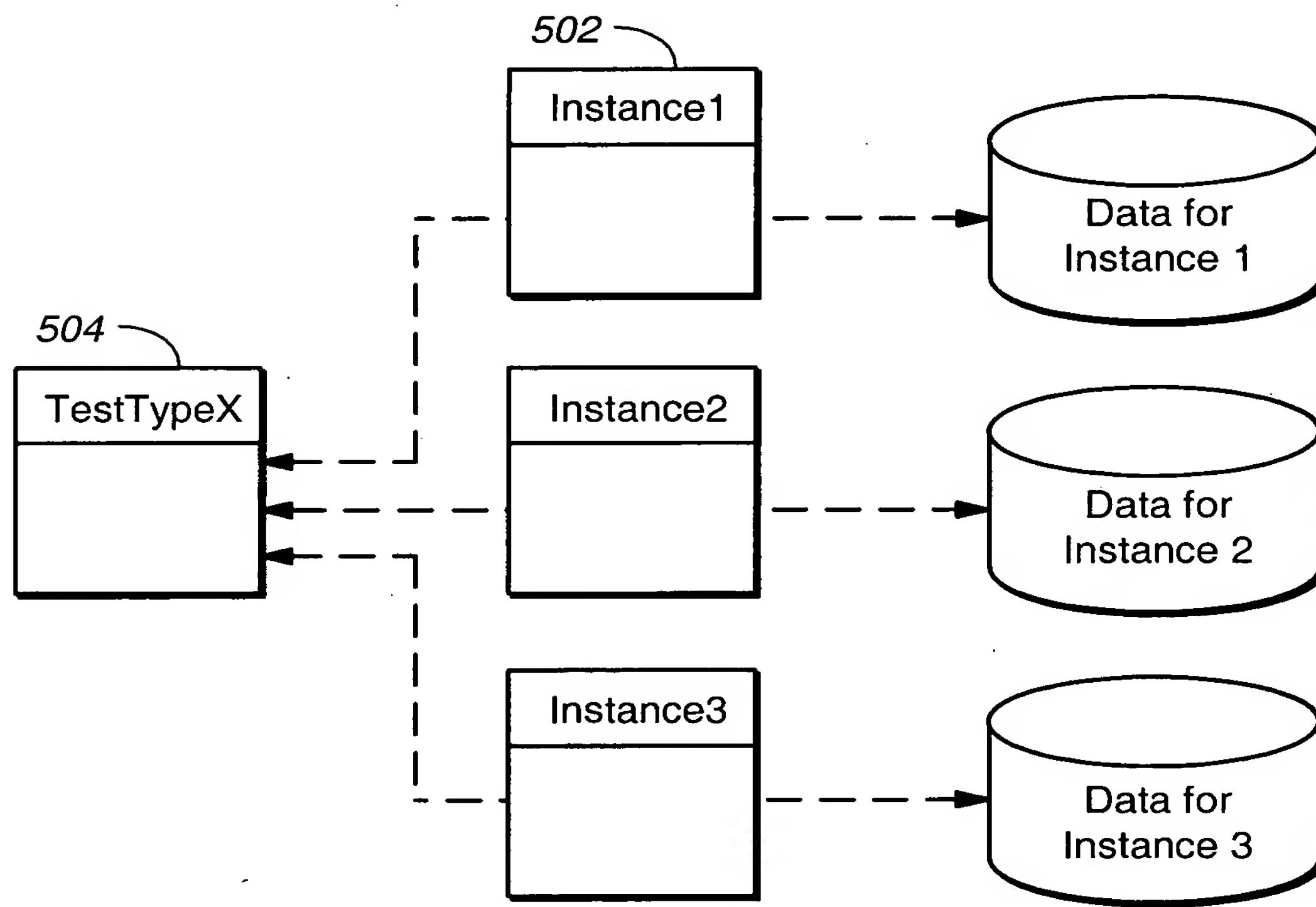
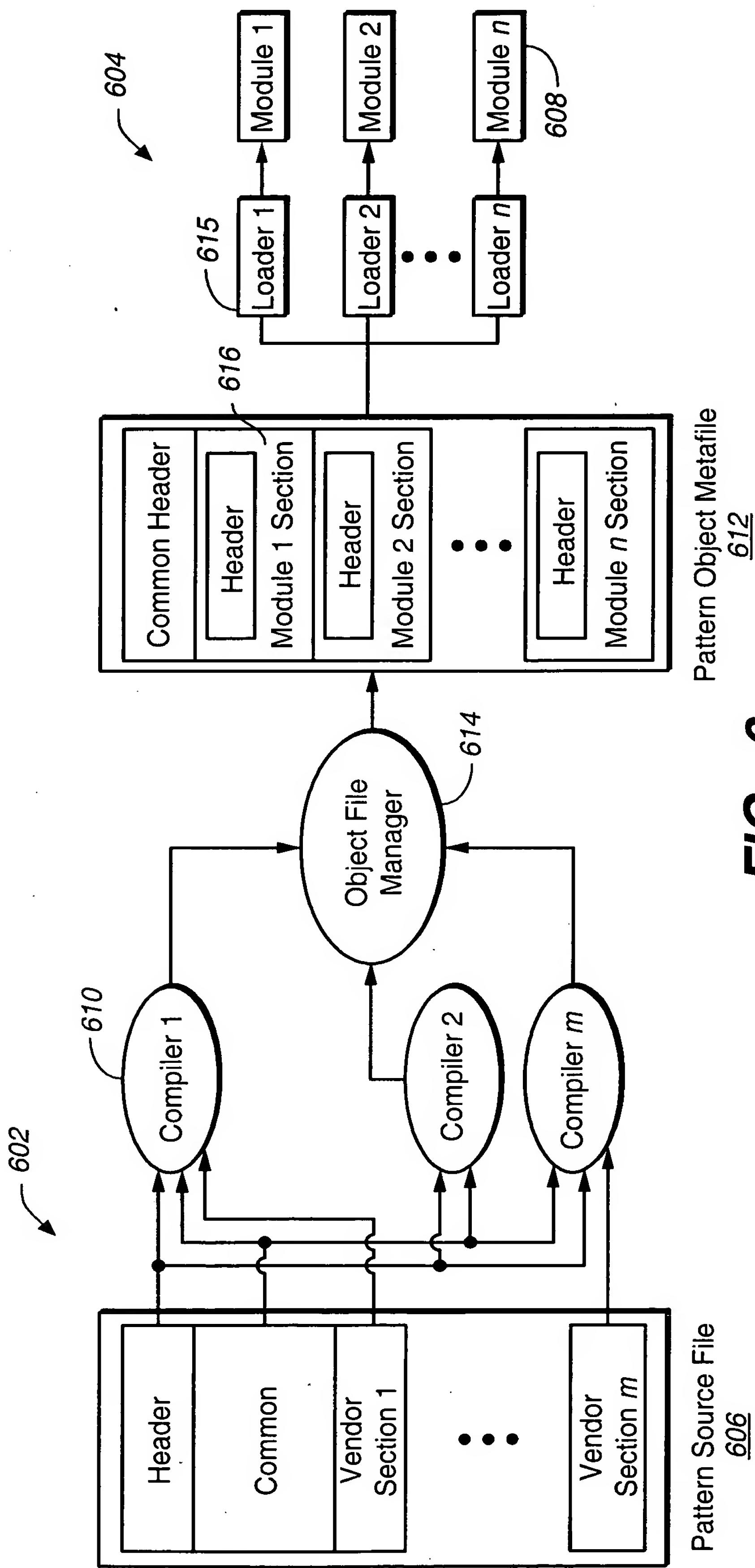


FIG._5



Pattern Source File
606

Pattern Object Metafile
612

FIG._6

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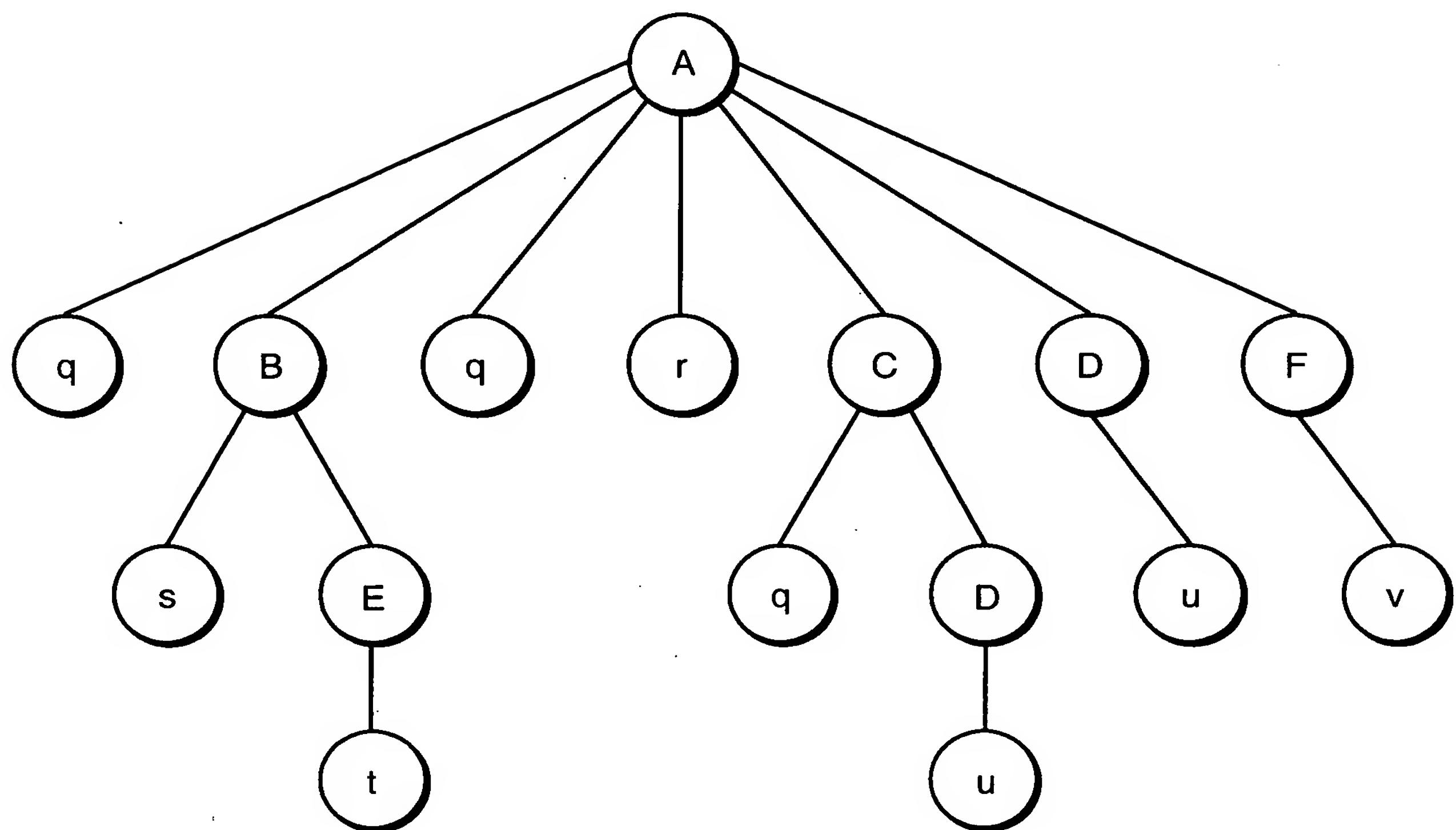


FIG._7

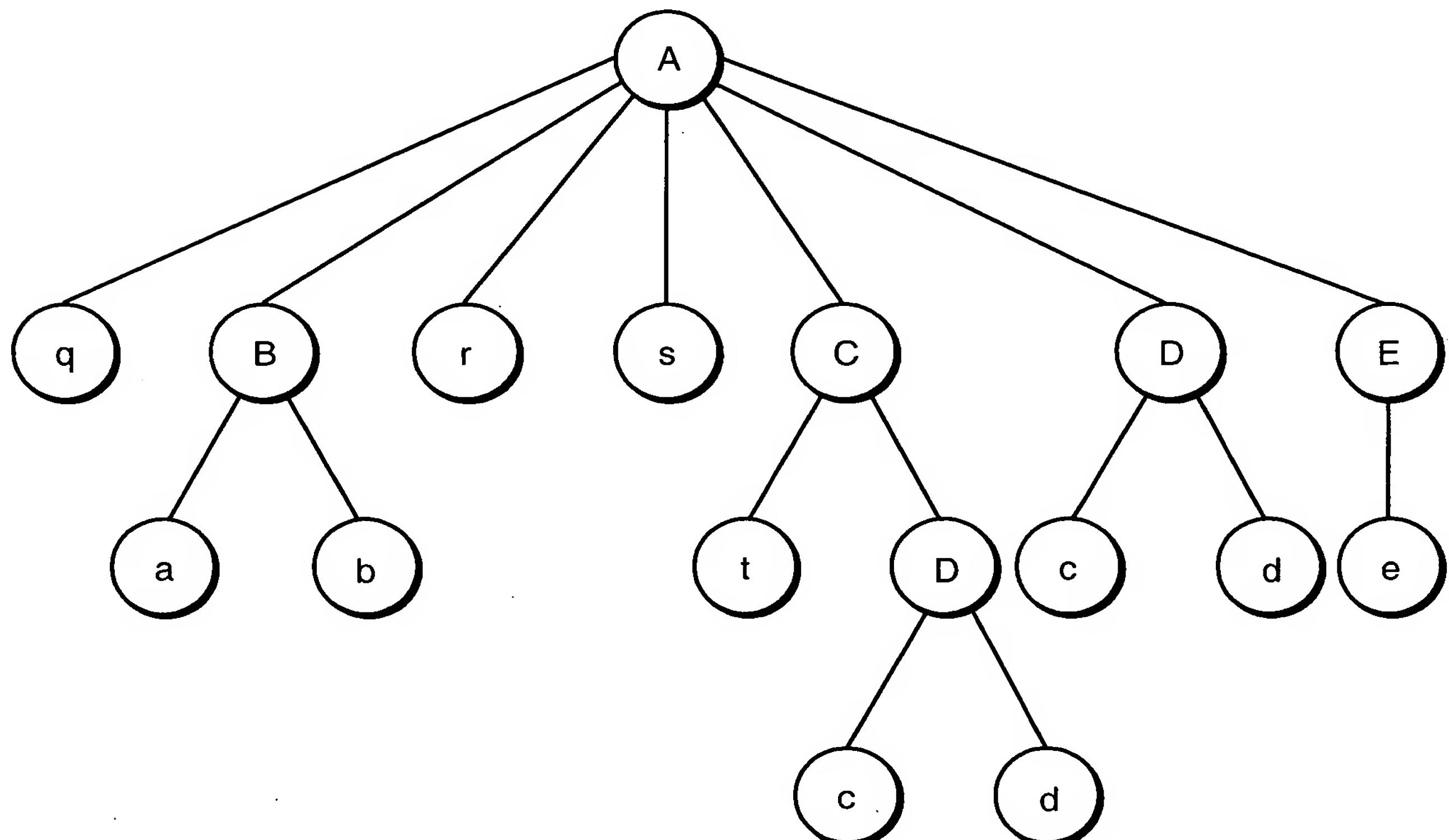


FIG._8

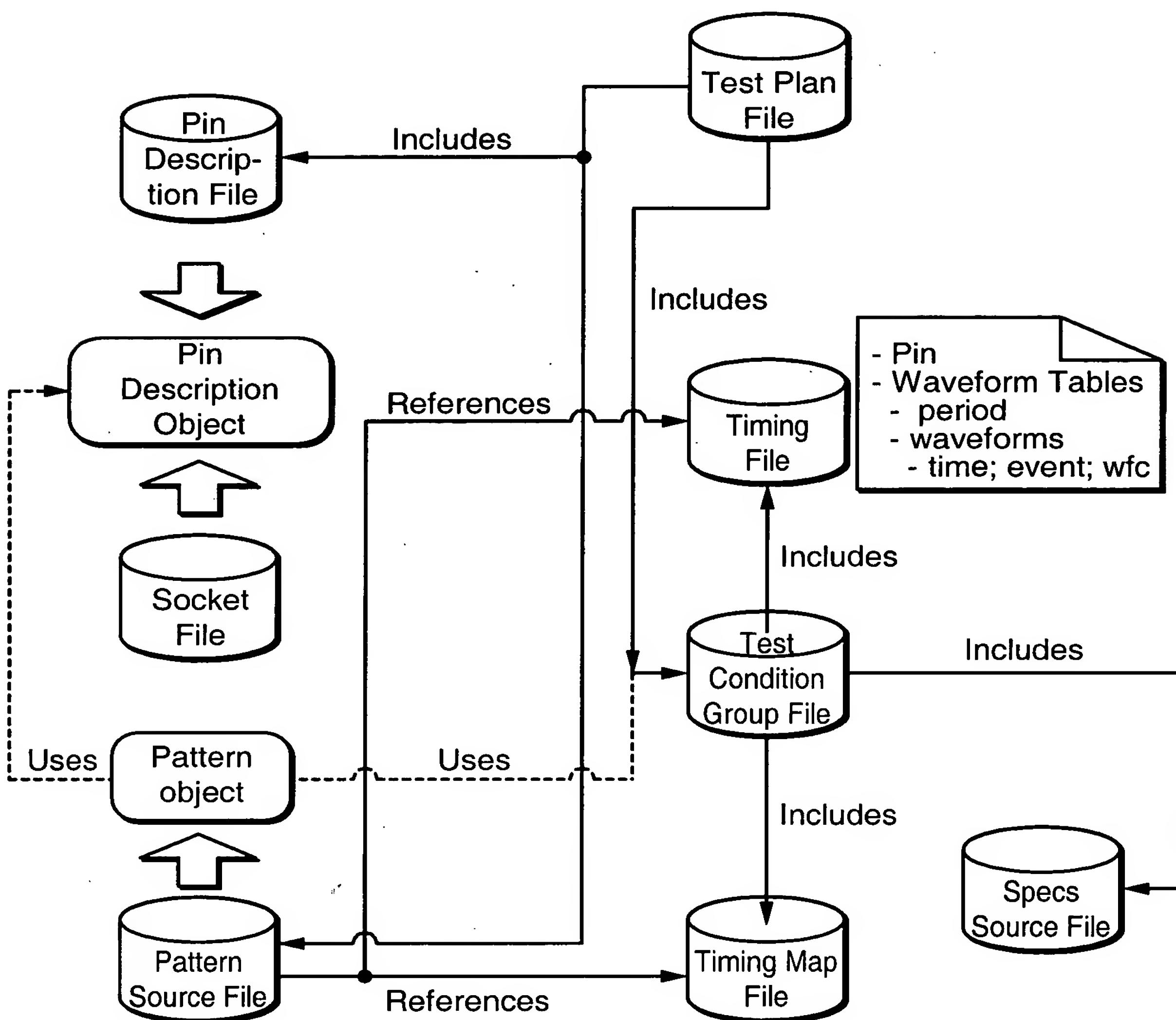


FIG._9

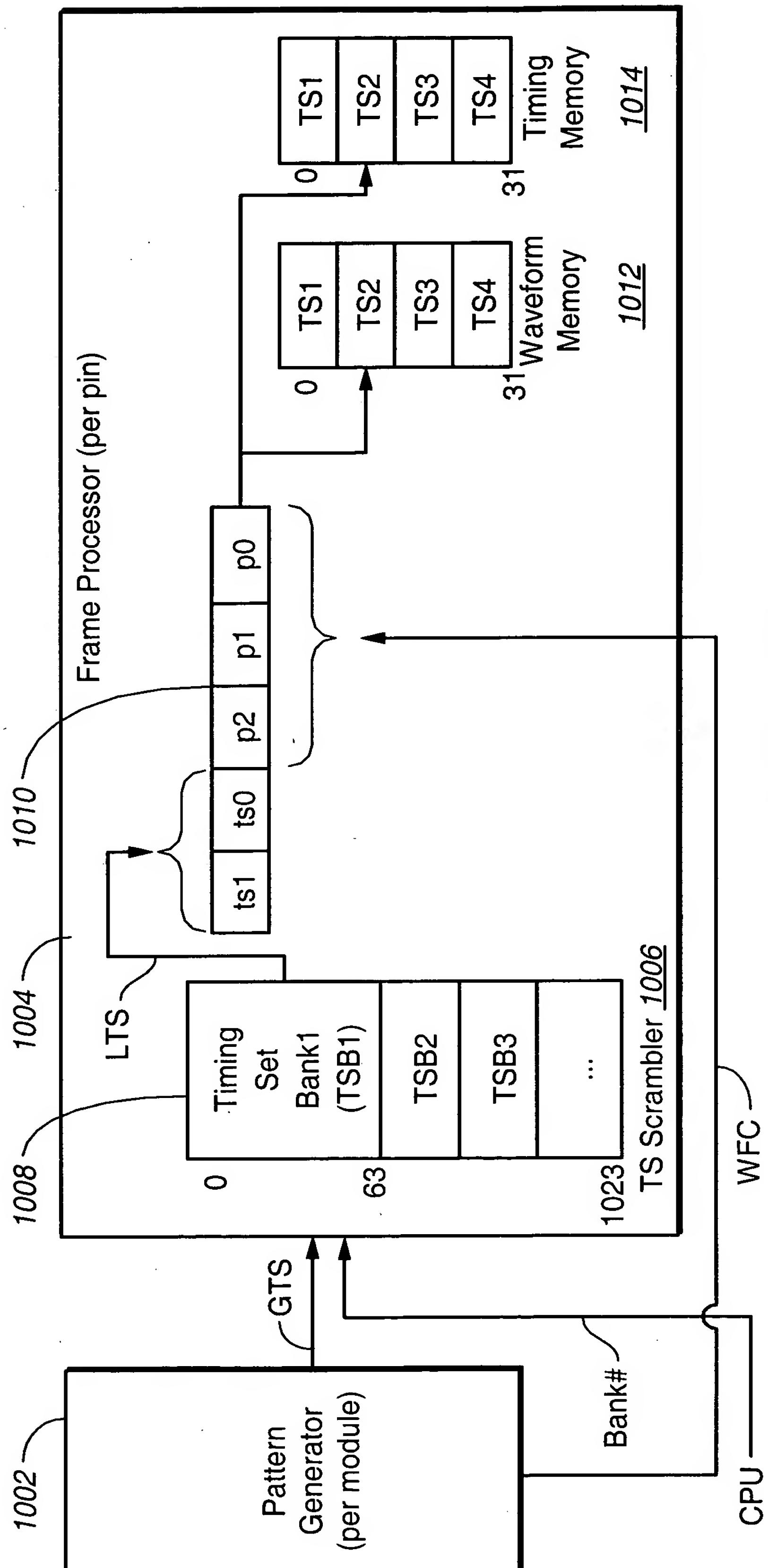


FIG.- 10

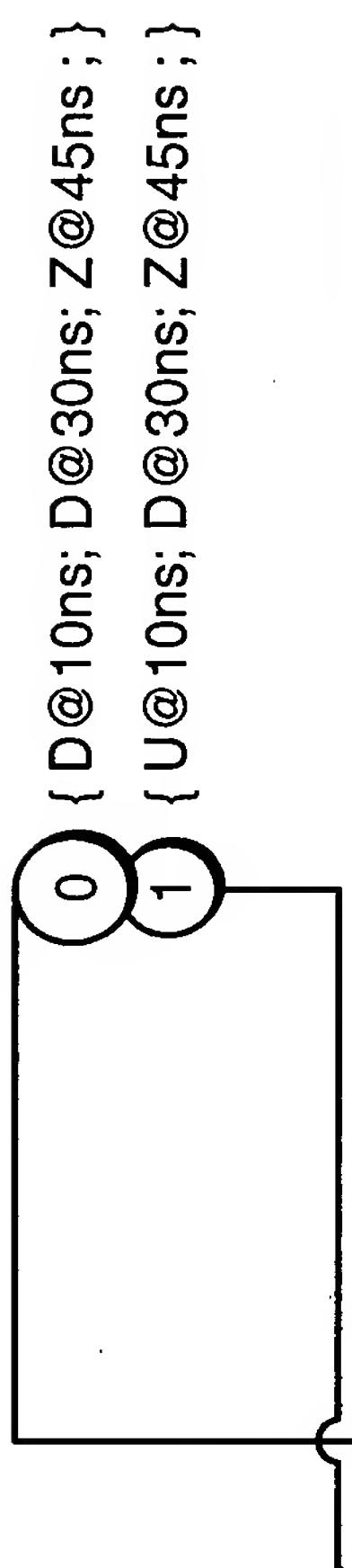
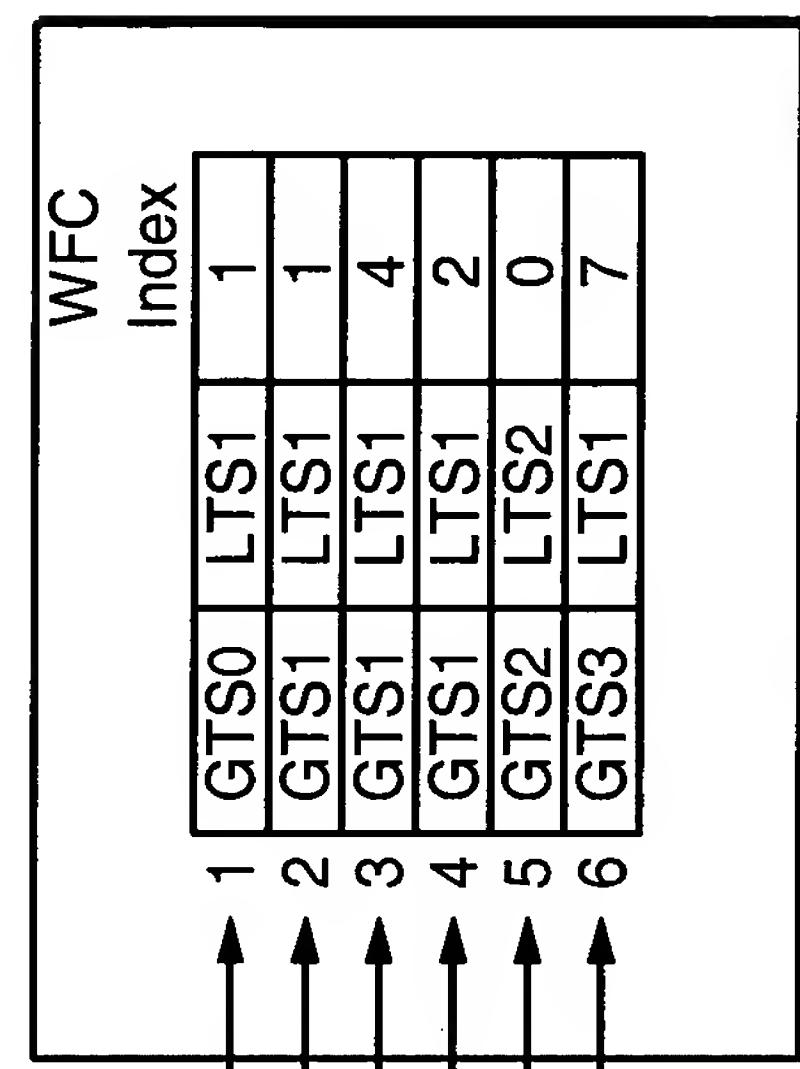


FIG.- 11



NOP V{SIG=1;CLK=1}W{SIG=wfs1;CLK=wfs1}}	1	GTS0	LTS1
NOP W{SIG=wfs2;}	2	GTS1	LTS1
NOP V{SIG=L;}	3	GTS1	LTS1
NOP V{SIG=d;}	4	GTS1	LTS1
NOP V{SIG=0;}	5	GTS2	LTS2
NOP V{SIG=n;}	6	GTS3	LTS1

FIG.- 12